POWER OPTIMIZED FM0/MANCHESTER ENCODER USING SOLS AND CLOCK GATING TECHNIQUE

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ABSTRACT:
The main objective of this project is to design a low power and reusable FM0/Manchester encoder for DSRC applications. Fully reused VLSI architecture using (similarity-oriented logic simplification) SOLS technique for both FM0 and Manchester encodings are proposed. Dedicated short-range communication is one-way or two-way short-range to medium-range wireless communication channels specifically designed for automotive use and a corresponding set of protocols and standards. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. Further, this project is enhanced by using clock gating technique to reduce the power consumption in memory organization. The power supply will be provided for corresponding accessed rows only. We have carried the simulation and verified the results using ISE simulator and synthesis is done on the XILINX ISE.

KEYWORDS: DSRC (Dedicated Short range Communication), SOLS (similarity oriented logic simplification), FM0, Manchester, gated clock, ring counter.

I. INTRODUCTION
FM0 and Manchester coding techniques are used to encode the data while transmit the signal through medium. Using similarities in the FM0 and Manchester coding, we developed the reused VLSI hardware architecture. Since, encoding plays a vital role in secured communication. Developing architecture of such encoding techniques is needed of the hour. One sort of renowned and commonly used communication technique is DSRC (Dedicated Short Range Communication), which is designed to support the variety of applications based on vehicular environment communication. DSRC is the subset of RFID (Radio Frequency Identification) for tracking and identification. SRC standards adopt both FM0 and Manchester encodings for signal reliability and dc balance.

Coding principles of FM0 and Manchester encoders:
The coding principles of FM0 and Manchester encoders are discussed as follows.

1. FM0 encoding:
FM0 encoding is also called as bi-phase space encoding scheme. In FM0 encoding, the signal to be transmitted according to the following rules: It inverts the phase of the baseband signal at the boundary of each symbol.
- For representing logic ‘0’ level, it inverts the signal at the mid of the symbol.
- For representing logic ‘1’ level, it constant voltage occupying an entire bit window.

2. Manchester encoding:
The Manchester encoding is obtained by performing XOR operation in between the clock

![Example for FM0 coding](image-url)
The coding examples of FM0 and Manchester are shown in fig. 1. The only one next-state that can satisfy both rules for the X of logic-1 is S4.

Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also construct the transition table of each state A(t) and B(t) represent the discrete-time state code of current state at time instant. Their previous-states are denoted as the A(t − 1) and the B(t − 1) respectively.

<table>
<thead>
<tr>
<th>Previous state</th>
<th>Current state</th>
</tr>
</thead>
<tbody>
<tr>
<td>A(t-1)</td>
<td>B(t-1)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1. Transition table of FM0.

With this transition table, the Boolean functions of A(t) and B(t) are given as:

\[ A(t) = B(t-1) \] ………(1)
\[ B(t) = X \oplus B(t-1) \] ……… (2)

Now the Boolean function of FM0 code can be denoted by using the above equations (1) and (2)

\[ \text{CLK } A(t) + \text{CLK } B(t) \] …………(3)

Now construct the hardware architecture of the fm0/Manchester encoder as shown in fig. 3.

Fig. 3. Hardware architecture of FM0 and Manchester encoders
The top part is denoted the fm0 code and then the bottom part is denoted the Manchester code. In fm0 code the DFFA and DFFB are used to store the state code of the fm0 code. Mux_1 and not gate is also used in the fm0 code. The Manchester code is obtained by using the XOR gate. When mode=0 the mux_2 selects fm0 code and mode=1 the mux_2 selects Manchester code as shown in fig.

### III. FM0 AND MANCHESTER ENCODER USING SOLS TECHNIQUE

To reduce the components used in FM0/Manchester encoder we are using SOLS (Similarity Oriented Logic Simplification) technique. The SOLS technique is classified into two parts: area compact retiming and balance logic operation sharing.

#### 1. Area compact retiming:

For fm0 the state code of each state is stored in DFFA and DFFB. By observing the equations (1) and (2) we can say that the transition to state code is only depending on the previous state of B(t-1) instead of both A(t-1) and B(t-1). So FM0 encoder requires only one flipflop to store B(t-1). But if the DFFA is removed then there is a problem with non-synchronization between A(t) and B(t) and hence causes logic fault. That’s why the DFFB is relocated after mux-1 as shown in fig.5 to avoid the logic fault.

#### 2. Balance Logic Operation Sharing:

We know that Manchester encoding is obtained by using XOR gate. Now we replace this XOR gate with MUX. Because the FM0 and Manchester logics have a common point of the multiplexer. By using balance logic operation integrate X into A(t) and X. B(t). The A(t) can be derived from an inverter of B(t-1), and X is obtained by an inverter of X. The logic for A(t)/X can use the same inverter, and then a multiplexer is placed before the inverter to switch the operands of B(t-1) and X. The Mode indicates either FM0 or Manchester encoding is adopted. The same concept can also be applied to the logic for B(t)/X.

Hence the logic computation times between A(t)/X and B(t)/X is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR signals. Whether FM0 or Manchester code is adopted, even one logic component of the proposed VLSI architecture is not wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved.

The VLSI architecture of FM0 and Manchester encodings using SOLS technique is shown in fig.6.

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**Fig. 4** FM0 encoding without area compact retiming

**Fig. 5** FM0 encoding with area compact

**Fig. 6** VLSI architecture of FM0 and Manchester encodings using SOLS technique

The above architecture consumes more power since the clock distribution network of the memory unit after encoding process consumes nearly 70% of the total power consumed by the integrated circuit since this is the only signal which has the highest switching activity. So we are designing the memory unit with clock gating technique to reduce power consumption.
IV. MEMORY ORGANIZATION

**Fig. 7** Block diagram of memory organization with clock gating technique

**INPUT BUFFER:**
The input buffer is also commonly known as the input area or input block. When referring to computer memory, the input buffer is a location that holds all incoming information before it continues to the CPU for processing. Input buffer can also be used to describe various other hardware or software buffers used to store information before it is processed.

**Memory Block:**
(RAM) Random-access memory (RAM) is a form of computer data storage. Today, it takes the form of integrated circuits that allow stored data to be accessed in any order (that is, at random). "Random" refers to the idea that any piece of data can be returned to a constant time, regardless of its physical location and whether it is related to the previous piece of data.

**Ring Counter:**
A ring counter is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register. There are two types of ring counters: Straight ring counter or Overbeck counter connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. For example, in a 4-register one-hot counter, with initial register values of 1000, the repeating pattern is: 1000, 0100, 0010, 0001, 1000,... Note that one of the registers must be pre-loaded with a 1 (or 0) in order to operate properly.

**Clock gating technique:**
The purpose of clock gating is to shut down the clock of any component whenever it is not being used. If there is no need of switching some elements in the circuit, then clock is not supplied to those elements.

**Ring counter with clock gated by using R–S flip-flop:**

The above block diagram shows the power controlled Ring counter as shown in fig. 8.

We know that the only one DFF is activated during the operation of ring counter eventhough all the D flipflops consumes power. So power is wasted, hence by using clock gating technique we can reduce the power consumption. The total flipflops are divided into two blocks. Each block is having one SR FLIPFLOP controller. Then, a "gate" signal is used for each block to gate the frequently toggled clocked signal when the block can be inactive so that unnecessary power wasted in clock signal transitions is saved. The clock signal is gated by RS-flip flop. When the input of the first DFF in a block is forced, it sets the output of the RS-flip flop to "1" at the next clock edge. Thus, the incoming “1” can be trapped in that block and continue to propagate inside the block. On the other hand, the successful propagation of “1” to the first DFF in the next block can henceforth shut down the unnecessary clock signal in the current block.

V. SIMULATION RESULTS
SYNTHESIS:

The power consumption of ring counter with and without clock gating technique is shown in Table 2.

<table>
<thead>
<tr>
<th>Power consumption (mw)</th>
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<tbody>
<tr>
<td>Ring counter with out clock gating</td>
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<tr>
<td>Ring counter with clock gating</td>
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</table>

Table 2. Power consumption of Ring counter

VI. CONCLUSION

In this paper we reduce the both hardware utilization rate and power consumption. Using similarities in the FM0 encoding and Manchester encoding techniques, hardware architecture is to be developed. Manchester and FM0 coding are very popular codes, as these codes are level insensitive, self-clocking and they provide signal absence detection and having the encoding clock rate embedded within the transmitted data. They encode the data as 1’s and 0’s. FM0 and Manchester encoding architectures combined together to form efficient compact architecture through SOLS (Similarity Orientation Logic Simplification) technique. The SOLS technique is done on hardware utilization by means of two core techniques. They are namely area compact retiming and balance logic operation sharing (BLOS). The proposed system with clock gated by RSflipflop consumes less power than the system without clock gating technique. This deduced architecture of FM0 and Manchester coding would well support the DSRC standards.

REFERENCES


